REMARKS

Claims 1-10 are pending of which claim 1 is independent. Claim 6-10 have been withdrawn. In this Amendment, claim 1 has been amended. Support is found in, for example FIG. 3 and paragraphs [0024], [0026]-[0027] and [0044] of the application-as-published. Care has been exercised not to introduce new matter.

Rejections of Claims Under 35 U.S.C. § 102

Claims 1-5 were rejected under 35 U.S.C. § 102(e) as being anticipated by Nose et al. (U.S. Patent No. 6,819,311, hereinafter "Nose"). Claims 1-5 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kwon et al. (U.S. Patent No. 6,947,043, hereinafter "Kwon"). These rejections are respectfully traversed for the following reasons.

Amended claim 1, in pertinent part, recites as follows:

> "a reference voltage generator circuit, which comprises plural resistors connected in series between two voltages, generates plural reference voltages from connection points of the plural resistors, switches over the reference voltage either to an image display voltage or to a black display voltage, and outputs the switched reference voltage to plural wiring lines connected to the connection points; and
>
> a signal line drive IC, to which an image data signal and the reference voltage are inputted, and which outputs a voltage based on the reference voltage and the image data signal, to a data line of the liquid crystal panel."

An example of the claimed subject matter is disclosed in FIG. 3 and paragraphs [0024], [0026]-[0027] and [0044] of the application-as-published. The reference voltage generator circuit 301, which is comprised of resistors connected in series, outputs reference voltages 300 to the signal line drive IC 200. The reference voltages 300 are generated by switching over to a voltage indicating an image display voltage (V0~V6, V9~V15) or to a black display voltage (V7, V8). The signal line drive IC 200 are driven by an image data signal 400, a horizontal clock 401,

an output latch pulse 402, other control signal 403, and plural reference voltages 300 and outputs image write voltages to data lines 102.

Nose fails to disclose the limitations of claim 1.

While the Examiner equates Nose's voltage signal VD inputted on the data(signal) lines D1~Dm with the "reference voltage" of claim 1, the voltage signal VD corresponds to the "voltage" outputted to the "data line of the liquid crystal panel," rather than "the reference voltage," and Nose's voltages V0~V9 inputted to the signal line driving circuit correspond to the "reference voltage." (See Fig. 11) Nose, however, is silent on how the voltages V0~V9 are generated and any circuit or element which "comprises plural resistors connected in series between two voltages, generates plural reference voltages from connection points of the plural resistors, switches over the reference voltage either to an image display voltage or to a black display voltage, and outputs the switched reference voltage to plural wiring lines connected to the connection points," as required by claim 1. Moreover, Nose does not teach that the voltage signal VD, which is allegedly equitable to the "reference voltage," is generated by a circuit comprised of "plural resistors connected in series" to generate "plural reference voltages from connection points of the plural resistors" by "switch[es]ing over the reference voltage either to an image display voltage or to a black display voltage, and output[s]ting the switched reference voltage to plural wiring lines connected to the connection points," as required by claim 1.

Turning to Kwon, the data driver 200 supplies normal data or adjust data to the data line D1 to Dm. (See FIG. 2) Kwon does disclose neither on receiving plural reference voltages based on which the normal data or adjust data are generated, as admitted by the Examiner, nor on the "reference voltage generator circuit" comprised of plural resistors to generate "plural reference voltages from connection points of the plural resistors" by "switch[es]ing over the reference

voltage either to an image display voltage or to a black display voltage, and output[s]ting the switched reference voltage to plural wiring lines connected to the connection points," as required by claim 1. For this failure to disclose by Kwon, the Examiner averred the reference voltage generator circuit is known in the art. However, the Examiner never discharges his burden by relying solely on common knowledge in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. *In re Zurko*, 258 F.3d 1379, 1385, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001)

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), based on the foregoing, it is submitted that Nose and Kwon do not anticipate claim 1, nor any claim dependent thereon. Thus, claim 1 and claims dependent thereon are patentable over Nose and Kwon.

Conclusion

Upon entry of the above claim amendments, claims 1-5 remain active in this application. Applicant submits that all of the claims are in condition for allowance. Accordingly, this case should now be ready to pass to issue; and Applicant respectfully requests a prompt favorable reconsideration of this matter.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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